REMARKS/ARGUMENTS

Receipt of the Office action dated July 22, 2004 is hereby acknowledged. In that action the Examiner: 1) objected to the specification for various informalities; 2) objected to claims 5 and 33 for various informalities; 3) rejected claims 1-3, 5-6, 17, 19-20, 23-24, 45 and 49-50 as allegedly anticipated by Kelkar (U.S. Patent No. 5,663,991); 4) rejected claims 27-28 and 32 as allegedly obvious over Kelkar in view of Neudeck (U.S. Patent No. 5,701,335); 5) rejected claims 39-40, 44 and 53 as allegedly obvious over Kelkar in view of admitted prior art; and 6) indicated claims 33 and 34 would be allowable if re-written to overcome the minor rejections of the Office action.

With this Response, Applicants amend claims 19, 27, 32-33, 45 and 50, cancel claims 1-3, 5-6, 17, 39-41, 44 and 53, and present new claims 62-66. Reconsideration is respectfully requested.

I. AMENDMENTS TO THE SPECIFICATION

With this Response, Applicants amend the specification to note the patent number of the parent case, and to correct the informality noted by the Examiner. No new matter is presented by these amendments.

II. OBJECTIONS TO THE CLAIMS

In the Office action the Examiner objected to claims 5 and 33 for various informalities. With this Response, Applicants cancel claim 5, thus mooting the objection with respect to claim 5. Further, Applicants make the correction requested by the Examiner to claim 33. No new matter is submitted by this amendment.

III. ALLOWED CLAIMS

In the Office action dated July 22, 2004 the Examiner indicated that claims 33 and 34 would be allowable if the minor informality of claim 33 is corrected. With this Response, Applicants have made the minor amendment requested, and thus claims 33 and 34 should be in a condition for allowance.

IV. CLAIM REJECTIONS

A. Claim 19

Claim 19 stands rejected as allegedly anticipated by Kelkar. Applicants amend claim 19 to remove the "step" terminology for clarification.

Kelkar is directed to an integrated circuit chip having built-in self measurement for PLL jitter and phase error. (Kelkar, Title). While Kelkar discloses in Figure 6 creation of a plurality of "clock phases 82," the total delay of the delay line 83 (and thus the phase relationship of the clock phases) is fixed at one period of the test clock, with tuning only to compensate for process variations and temperature differences.

> **Thus, the calibration circuit works by forcing the total delay to be equal to one period of the test clock 84.**
> ...
> By using the calibration system, the total delay is automatically adjusted to the desired amount. Process variations as well as environmental differences in temperature and power supply voltage can be automatically tuned out using this calibration circuit.

(Kelkar, Col. 6, lines 4-35 (emphasis added)).

Claim 19, by contrast, specifically recites, "adjusting the time window; and repeating the comparing and adjusting to determine the uncertainty window." In Kelkar, any window defined between clock phases 82 remains constant, even in the face of process variations, temperature differences and/or power supply voltage swings. Kelkar fails to teach or fairly suggest that the time window defined between features of a first and second reference clock signal should be adjusted.

Based on the foregoing, Applicants respectfully submit that claim 19, and all claims which depend from claim 19 (claims 20 and 23-24), should be allowed.

B. Claim 27

Claim 27 stands rejected as allegedly obvious over Kelkar in view of Neudeck. Applicants amend claim 27 to remove the "adapted to" terminology.

Kelkar is directed to an integrated circuit chip having built-in self measurement for PLL jitter and phase error. (Kelkar, Title). While Kelkar

discloses in Figure 6 creation of a plurality of "clock phases 82," the total delay of the delay line 83 (and thus the phase relationship of the clock phases) is fixed at one period of the test clock, with tuning only to compensate for process variations and temperature differences. (Kelkar, Col. 6, lines 4-35). Neudeck appears to be directed to a frequency independent scan chain. (Neudec, Title).

Claim 27, by contrast, specifically recites, "wherein the external measurement system adjusts a phase relationship of a plurality reference clock signals having varying phase, the plurality of reference clock signals define a plurality of time windows between corresponding features ... ." As admitted in the Office action, Kelkar fails to teach an "external measurement system connected by way of a scan chain that executes software to control the measurement circuit and to adjust phase relationships... ." (Office action of July 22, 2004, page 6, paragraph 6). Further, in the Kelkar system the phase relationships of the clock phases are fixed. (Kelkar, Col. 6, lines 4-35). Because Kelkar does not adjust phase relationships, even if the teachings of Neudeck are precisely as the Office action suggests (which the Applicants do not admit) the combination still fails to teach an "external measurement system [that] adjusts a phase relationship of a plurality reference clock signals having varying phase."

Based on the foregoing, Applicants respectfully submit that claim 27, and all claims which depend from claim 27 (claims 28 and 32), should be allowed.

C. Claim 45

Claim 45 stands rejected as allegedly anticipated by Kelkar. Applicants amend claim 45 to remove the "step" terminology for clarification.

Kelkar is directed to an integrated circuit chip having built-in self measurement for PLL jitter and phase error. (Kelkar, Title). While Kelkar discloses in Figure 6 creation of a plurality of "clock phases 82," the total delay of the delay line 83 (and thus the phase relationship of the clock phases) is fixed at one period of the test clock, with tuning only to compensate for process variations and temperature differences. (Kelkar, Col. 6, lines 4-35).

Claim 45, by contrast, specifically recites, "adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width

of at least one time bin; and repeating the adjusting and the comparing until the uncertainty window is determined." In Kelkar, any window defined between clock phases 82 remains constant, even in the face of process variations, temperature differences and/or power supply voltage swings. Thus, Kelkar fails to teach or fairly suggest adjusting the time width of at least one time bin, or that the adjusting and the comparing should be repeated until the uncertainty window is determined.

Based on the foregoing, Applicants respectfully submit that claim 45, and all claims which depend from claim 45 (claims 49 and 50), should be allowed.

V. NEW CLAIMS

With this Response, Applicants present new claims 62-66. Applicants respectfully submit that these claims are not taught or rendered obvious by the related art.

VI. CLAIM CANCELLATIONS

With this Response, Applicants cancel claims 1-3, 5-6, 17, 39-41, 44 and 53. This cancellation is without prejudice to later asserting these claims, such as in a continuation.

VII. CONCLUSION

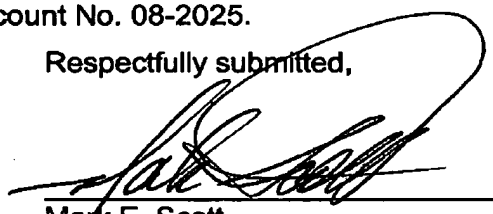
Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Appl. No. 10/655,321
Amdt. dated October 20, 2004
Reply to Office action of July 22, 2004

Applicants respectfully request that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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